

In the Claims:

Please amend the claims as follows:

1. (Canceled)
2. (Currently Amended) The adapter of Claim ~~1~~ 16 wherein the at least one first interconnect is physically spaced to correspond to a first pin configuration of a power module.
3. (Currently Amended) The adapter of Claim ~~1~~ 16 wherein the at least one second interconnect is physically spaced to correspond to a second pin configuration of an end user's circuit board.
4. (Currently Amended) The adapter of Claim ~~1~~ 16 wherein a signal modifying circuit acts upon an input to the adapter.
5. (Currently Amended) The adapter of Claim ~~1~~ 16 wherein a signal modifying circuit acts upon an output to the adapter.
6. (Original) The adapter of Claim 2 wherein the power module is a DC-to-DC converter.
7. (Original) The adapter of Claim 2 wherein the power module is an AC-to-DC converter.
8. (Original) The adapter of Claim 2 wherein the power module is a DC-to-AC inverter.
9. (Currently Amended) The adapter of Claim ~~1~~ 16 wherein the first interconnects comprise surface mount connects.
10. (Currently Amended) The adapter of Claim ~~1~~ 16 wherein the first interconnects comprise through hole connects.
11. (Canceled)

12. (Canceled)

13. (Currently Amended) The adapter of Claim ~~1~~ 16 wherein the signal modifying circuit comprises a filter.

14. (Currently Amended) The adapter of Claim ~~1~~ 16 wherein the signal modifying circuit comprises an overvoltage protection device.

15. (Currently Amended) The adapter of Claim ~~1~~ 16, further comprising:

- (a) at least a second interconnect on the first surface,
- (b) at least one connective path between the first interconnect on the first surface and the second interconnect on the first surface, and
- (c) a signal modifying circuit between the first interconnect on the first surface and the second interconnect on the first surface.

16. (Currently Amended) ~~The adapter of Claim 1, further comprising:~~

An adapter comprising:

- (a) a first and a second surface;
- (b) at least one first interconnect on the first surface;
- (c) at least one second interconnect on the second surface, the at least one second interconnect comprising a through hole connect;
- (d) at least one connective path between the first and second interconnects;
- (e) a signal modifying circuit between the first interconnect and the second interconnect;
- ~~(a)~~ (f) at least a second interconnect on the second surface,
- ~~(b)~~ (g) at least one connective path between the first interconnect on the second surface and the second interconnect on the second surface, and
- ~~(c)~~ (h) a signal modifying circuit between the first interconnect on the second surface and the second interconnect on the second surface.